Remarks

The present amendment responds to the final Official Action dated August 22, 2005. The Official Action rejected claims 34 and 53 based on the judicially created doctrine of obviousness-type double patenting over claims 1 and 9 of U.S. Patent No. 6,366,999. Claims 34-40, 53, and 56-61 were rejected under 35 U.S.C. §103(a) based on Dibrino et al. U.S. Patent No. 6,061,707 (Dibrino) in view of Pawate et al. U.S. Patent No. 5,528,550 (Pawate). Claims 62, 64, and 65 were rejected under 35 U.S.C. §102(e) as being anticipated by Dibrino. Claims 63 and 66 were rejected under 35 U.S.C. §103(a) based on Dibrino in view of Pawate. These grounds of rejection are addressed below.

A terminal disclaimer to obviate the provisional double patenting rejection is being filed with this response. Authorization to charge Deposit Account No. 50-1058 for the terminal disclaimer fee of $130 under 37 C.F.R. §1.20(d) accompanies this response. Claims 1-33 and 41-52 have been previously cancelled. Claims 34-40 and 53-66 are presently pending.

Interview Summary

The Examiner is thanked for the courtesy of a telephone interview concerning the above case on October 3, 2005. Dr. Pechanek, a co-inventor of the present application, and the undersigned attorney were involved in the telephone call. In the telephone call, the three points found at paragraphs 12, 13, and 14 in the Official Action were discussed.

As an initial matter, Applicants' representatives explained how each claimed term of claim 34 corresponds with Fig. 5A of the present application and how the claimed invention

addresses conditional execution of instructions by storing arithmetic condition flags (ACFs) and controlling the ACFs with instructions.

In reply to the first point found at paragraph 12, it was pointed out that the operands 11 and 12 in Fig. 2 of Dibrino, upon which the Official Action relied, terminate as inputs to bit shifter 23 and carry and save adder 24, respectively. These operands are not connected to a control input of any element in Fig. 2 of Dibrino and, thus, cannot control conditional execution as claimed. Furthermore, the text at col. 3, lines 17-29 of Dibrino was also discussed. The Examiner relied on this cited portion of text in an earlier Official Action for purportedly suggesting the claimed feature "control lines derived from a registered instruction in a processor pipeline," as claimed in claims 34 and 53. This text was reviewed with the Examiner and it was agreed that there is no mention of "control lines" and no mention of "control lines derived from a registered instruction" found in the text. Consequently, Applicants urge that Dibrino does not teach and does not suggest "instruction control lines derived from a registered instruction in a processor pipeline, the instruction control lines including conditional execution control lines to control conditional operation as specified in an instruction", as claimed in claims 34 and 53. See also claim 62.

In reply to the second point found at paragraph 13, Applicants' representatives explained that the carry input to AND gate 27 and the shift count output to AND gate 27 of Fig. 2 of Dibrino were not equivalent to the claim limitation "an arithmetic condition flag (ACF) generation unit for providing a Boolean combination of a present selected state with a previous state," as claimed in claim 34. Dibrino's AND gate 27 performs a Boolean AND operation but

does not contain or connect a latch to perform a Boolean combination of a present selected state with a previous state. Claim 34 claims coupling the ACF generation unit to a latch when it recites "an ACF latch for storing the previous state and feeding the previous state back to the ACF generation unit." Furthermore, the carry input of Dibrino is a resultant of an arithmetic unit such as elements 32 and 34 of Fig. 3 of Dibrino. As a resultant of an arithmetic unit, the carry input is more similar, but still distinct in other ways, to a different element of claim 34, the separately claimed element "arithmetic scalar condition state."

The Examiner agreed to re-review Dibrino, in light of the telephone interview, and withdraw the rejections based on Dibrino if, after his re-review, he confirms that Dibrino does not teach or suggest "control lines derived from a registered instruction."

In reply to the third point found at paragraph 14 where the Official Action states that the "applicant did not explain why he thought that Pawate did not disclosed [sic] ACF latch for storing previous state and feeding previous state back to the ACF generation unit," Applicants' representatives explained that it is not the burden of the Applicants to show why a claim element is not disclosed. Rather, it's the burden of the Examiner to determine whether an element in a claim is disclosed by a reference.

Applicants' representatives also explained that even if the accumulator 62 of Fig. 3 of Pawate included a latch, which Applicants believe it does not, the feedback path between the accumulator 62 and ALU 60 is a data path for accumulating a data operation. Pawate, col. 5, lines 30-32. In contrast to Pawate, the ACF latch as claimed in claims 34 and 53 is in a control path and not in the data path. The data path of Fig. 5A of the present application is denoted by

element number 515. Consequently, Pawate's accumulator 62 and ALU 60 fail to teach and fail to suggest "an ACF latch for storing the previous state and feeding the previous state back to the ACF generation unit," as claimed in claim 34.

The Examiner agreed to re-review Pawate, in light of the telephone call, and withdraw the rejections based on Pawate if, after his re-review, he confirms that Pawate accumulator 62 differs from the ACF latch as claimed. Applicants also noted that there are multiple latches in claim 34 and the coupling to such latches are also claimed. For example, claim 34 recites "a second latch connected to the conditional execution control lines for holding instruction control signals for the instruction after the instruction has finished its execution state." Applicants urge the Examiner to interpret the claims as a whole. Even if latches are disclosed in the relied upon art or other art, for that matter, Applicants believe the art does not disclose latches advantageously connected in the manner claimed.

The Art Rejections

For conciseness and in light of the Examiner Interview summarized above, it is noted that the detailed analysis of the Art Rejections section of the response filed June 17, 2005, applies here as well. Rather than repeat it here, it is incorporated by reference herein in its entirety and should be considered by the Examiner. Further, the Examiner should not hesitate to call the undersigned should any questions arise.

Conclusion

All of the presently pending claims, as amended, appearing to define over the applied references, withdrawal of the present rejection and prompt allowance are requested.

Respectfully submitted,

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